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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,957	PANDE, ANAND	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *20-22,25 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory FRITZ FLEMING PRIMARY EXAMINER 4/18/2006 GROUP 2100 AU 2181

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 19, and 23 – 24 have been examined. Claims 20 – 22 and 25 – 26 have been withdrawn from consideration because of a previous restriction requirement.

Response to Arguments

2. Applicant's arguments filed 14 February 2006 have been fully considered but they are not persuasive.

As per Applicants arguments to the rejection of claim 1, Applicant argues that the combination of US Patent No. 6,337,893 (hereinafter Pontius) in view of US Patent No. 6,703,950 (hereinafter Yi) is improper. Applicant argues that Pontius teaches using a reduced Gray code that must have (1) bilateral translation symmetry and (2) bilateral reflective symmetry (14 February 2006 Amendment; Page 7 Paragraph 9). Applicant argues that Yi teaches only using a Gray code with bilateral reflective symmetry and not bilateral translation symmetry (14 February 2006 Amendment; Page 7 Paragraph 8). Applicant argues that since the two references teach using Grey codes with different bilateral symmetry, it is improper to combine the references because the change in Gray code symmetry would change the principle of operation of Pontius (14 February 2006 Amendment; Page 8 Paragraph 3). The Examiner argues that Pontius teaches using a Gray code with only bilateral reflective symmetry and also notes that using such a Gray code has an advantage of only requiring one skip, which simplifies the incrementer design (Pontius; Col 8 Lines 6 – 12). Therefore, the combination of the two

references, Pontius and Yi, does not depart from the principle of operation of Pontius and is proper.

As per Applicants arguments to the rejection of claims 5 – 11, 14, 15, and 17 – 19, Applicant argues that the combination of Pontius in view of Yi, and in further view of US Patent No. 6,810,468 (hereinafter Miyamoto) is improper because the references teach away from each other (14 February 2006 Amendment; Page 6 Paragraph 6). Applicant suggests that Yi's teaching that full-length sequences is wasteful (Yi; Col 2 Lines 33 – 42) teaches away from Miyamoto's teaching of a FIFO circuit with a memory having addresses for 2^N words where N is an integer (Miyamoto; Col 2 Lines 51 – 53, Col 3 Lines 55 – 56) (14 February 2006 Amendment; Page 6 Paragraphs 6 and 7). Applicant also suggests that Pontius teaches away from Miyamoto because Pontius suggests that FIFOs with 2^N depth have excess capacity (Pontius; Col 2 Lines 58 – 61) (14 February 2006 Amendment; Page 6 Paragraph 9). The Examiner argues that the teachings of Pontius and Yi do not teach away from those of Miyamoto, but are merely ordinary engineering design considerations. The excess capacity and wastefulness of 2^N depth FIFOs is an ordinary consideration when trying to balance capacity, space, and cost in the design of a system. Therefore Pontius and Yi do not teach away from Miyamoto, and the combination of the three references is proper.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 4, 12 – 13, 16, and 23 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,337,893 (hereinafter Pontius) in view of US Patent No. 6,703,950 (hereinafter Yi).

As per claim 1, Pontius teaches a first-in-first-out (FIFO) memory having a length of d where d is an integer (Pontius; Col 4 Lines 37 – 46). Pontius also teaches generating a code sequence having a length of 2d (Pontius; Col 4 Lines 37 – 46).

Pontius does not teach that the code sequence is a first code sequence and is generated from a second code sequence by removing one or more pairs of mirrored codes from the second code sequence. The first code sequence has a circular property and a Hamming length of one for any two consecutive codes of the first code sequence.

However, Yi teaches producing a code sequence of any even integer length and having a circular property and a Hamming length of one for any two consecutive codes by reducing a second code sequence (Yi; Figure 3a, Table 3a) into a first code sequence (Yi; Figure 3b, Table 3b) by removing one or more pairs of mirrored codes from the second code sequence (Yi; Figures 3a – 3b, Tables 3a – 3b, and Col 4 Lines 5 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings Pontius to include wherein the code sequence is generated by removing one or more pairs of mirrored codes from a second code sequence to form a first code sequence that has a length of 2d, a circular property, and a Hamming length of one for any two consecutive codes because doing so allows for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58).

As per claim 2, Yi also teaches wherein the second code sequence has a circular property and a Hamming length of one for any two consecutive codes of the second code sequence (Yi; Figures 3a – 3b).

As per claim 3, Yi also teaches wherein the first code sequence is a Gray-code sequence (Yi; Figures 3a – 3b).

As per claim 4, Yi also teaches wherein the second code sequence is a Gray-code sequence (Yi; Figures 3a – 3b).

As per claim 12, Pontius and Yi also obviously teach wherein the FIFO memory comprises a write data input port and a read data input port because these ports are common on FIFO memory devices.

As per claim 13, Pontius and Yi also obviously teach wherein the FIFO memory comprises a write pointer input and a read pointer input because these inputs are common on FIFO memory devices.

As per claims 16 and 23, Pontius teaches a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers (Pontius; Col 4 Lines 37 – 46). A code sequence of length 2d is generated and used as read and write pointers to the memory (Pontius; Figure 1 Items 10 and 20, Col 4 Lines 37 – 46).

Pontius does not teach reducing a first Gray-code sequence of length 2^n into a second Gray-code sequence of length 2d by removing one or more pairs of mirrored Gray-code sequences.

However, Yi teaches reducing a first Gray-code sequence of length 2^n (Yi; Figure 3a, Table 3a) into a second Gray-code sequence of length 2d (Yi; Figure 3b, Table 3b) by removing one or more pairs of mirrored Gray-codes from the first Gray-code sequence (Yi; Figures 3a – 3b, Tables 3a – 3b, and Col 4 Lines 5 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pontius to include wherein a Gray-code sequence of length 2^n is reduced into a Gray-code sequence of 2d by removing one or more pairs of mirrored Gray-code sequences from the first Gray-code sequence because doing so allows for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58).

As per claim 24, Yi also teaches wherein at least one of the first code sequence and the second code sequence has at least one of a closed property and a Hamming distance of one (Yi; Figures 3a – 3b).

4. Claims 5 – 11, 14 – 15, and 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,337,893 (hereinafter Pontius) in view of US Patent No. 6,703,950 (hereinafter Yi) as applied to claims 1 – 4, 12 – 13, 16, and 23 – 24 above, and further in view of US Patent No. 6,810,468 (hereinafter Miyamoto).

As per claim 5, Pontius in combination with Yi teaches the data structure as described per claim 1 (see rejection of claim 1 above).

Pontius in combination with Yi does not teach that the code generator is coupled to a write pointer that is in turn connected to the first-in-first-out (FIFO) memory.

Miyamoto teaches an asynchronous FIFO memory that has a code generator connected to a write pointer (Miyamoto; Figure 1 Item 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Pontius in combination with Yi to include a write pointer that is connected to the code generator and the FIFO memory because doing so allows for determination of asynchronous FIFO status flags without stability errors.

As per claim 6, Miyamoto also teaches wherein the write pointer is coupled to the FIFO memory via at least one of a converter and a look-up table (Miyamoto; Figure 1 Item 21c).

As per claim 7, Miyamoto also teaches wherein the converter comprises a Gray-to-Binary converter (Miyamoto; Figure 1 Item 21c).

As per claim 8, Miyamoto also teaches wherein the code generator is coupled to a read pointer (Miyamoto; Figure 1 Item 22), which in turn is connected to the FIFO memory.

As per claim 9, Miyamoto also teaches wherein the read pointer is coupled to the FIFO memory via a Gray-to-binary converter (Miyamoto; Figure 1 Item 22c).

As per claim 10, Miyamoto also teaches wherein the code generator is coupled to a read pointer (Miyamoto; Figure 1 Item 22), which in turn, is coupled to the storage device.

As per claim 11, Pontius in combination with Yi and Miyamoto also obviously teaches wherein the storage device comprises a bank of registers because a bank of registers can store information the same way as a FIFO memory device.

As per claim 14, Pontius in combination with Yi and Miyamoto also obviously teaches that the asynchronous FIFO memory comprises a write clock domain and a read clock domain because asynchronous memory devices typically have a read clock domain and an independent write clock domain.

As per claim 15, Pontius in combination with Yi and Miyamoto also obviously teaches that the asynchronous FIFO memory comprises a write clock in the write clock domain, a read clock in the read clock domain, and that the read and write clock are asynchronous to each other because any asynchronous system has separate independent clocks to perform separate operations in different domains that are independently from one another.

As per claim 17, Miyamoto also teaches that reading and writing are asynchronous (Miyamoto; Col 3 Lines 34 – 37).

As per claim 18, Pontius and Miyamoto also teach that reading and writing are part of a FIFO process (Pontius; Col 4 Lines 37 – 46) (Miyamoto; Col 3 Lines 34 – 37).

As per claim 19, Pontius and Miyamoto also teach that the asynchronous memory is an asynchronous FIFO memory (Pontius; Col 4 Lines 37 – 46) (Miyamoto; Col 3 Lines 34 – 37).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard Franklin
Patent Examiner
Art Unit 2181

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181

4/28/2006